



8/Response
by
CBR

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Shinichi Yoshimura et al.

Appl. No.: 10/009,857

Conf. No.: 6313

Filed: May 6, 2002

Title: PICTURE PROCESSING APPARATUS AND PHOTOGRAPHING DEVICE

Art Unit: 2676

Examiner: Tam D. Tran

Docket No.: 113278-007

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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MAY 28 2004

Technology Center 2600

RESPONSE TO OFFICE ACTION

Sir:

The present remarks are in Response to the Non-Final Office Action entered in the above-identified case and mailed on January 21, 2004. Claims 16-33 are pending in the application. All stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,079,624 to Sasuga. Applicants respectfully traverse.

Claims 16, 22 and 28 are the only independent claims pending in the instant application. Each of the independent claims relates to one or more pixels in a picture processing apparatus or photographic device. Each of the independent claims call for, among other things, "a plurality of storing portions, wherein each storing portion stores, as a current signal, [an] electric signal amplified by [an] electric signal amplified by [an] amplifying portion, and a load portion for converting the current signal stored by each storing portion into a voltage signal. Sasuga et al. do not disclose a plurality of storage areas for storing an amplified electric signal as a current signal as required by the independent claims, no do they teach a load portion for converting such stored current signals into a voltage signals.

The Examiner points to Sasuga et al. col. 33, lines 8-15 as teaching a plurality of storing portion for storing the amplified electric signal as a current signal, but the cited passage merely identified varies types of binary memories. Nothing in cited passage indicates that the memories are provided to store an amplified electric signal that represents the intensity of light received by a light receiving portion, as a current signal. The memories described in column 33, lines 8-15

are binary, or digital memories. Such memories are not configured to store a current signal as required by the claims. This fact is emphasized by the passage cited by the Examiner at column 44, lines 54-67. "The output of line sensor 226 is amplified by amplifier 231 and is then converted into a digital signal, which in turn is converted by A/D converter 235 into a density signal. Clearly this signal is not a current signal as called for in the claims. Furthermore the Examiner points to the A/D converter 235 as teaching the load portion of the pending is provided for converting current signals stored in the storing portions into a voltage signal. Whereas the A/D converter 235 taught by Sasuga et al. converts an awards signal (be it a voltage signal or a current signal) into a digital signal. This simply is not what is being claimed in the present application. Since Sasuga et al. do not teach all of the elements of any of the independent claims pending in the instant application. The rejection under 35 U.S.C. §102(b) is improper and should be withdrawn.

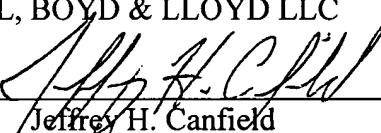
For these reasons, Applicant respectfully submits that the claims as presently amended are all in condition for allowance. Applicant therefore requests that the Examiner allow the claims move the application to issue. However, if there are any remaining issues the Examiner is encouraged to call Applicants' attorney, Jeffrey H. Canfield at (312) 807-4233 in order to facilitate a speedy disposition of the present case.

If any additional fees are required in connection with this response they may be charged to deposit account no. 02-1818.

Respectfully submitted,

BELL, BOYD & LLOYD LLC

BY



Jeffrey H. Canfield

Reg. No. 38,404

P.O. Box 1135

Chicago, Illinois 60690-1135

Phone: (312) 807-4233

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